GRAFONICS :
Graphène Fonctionnalisé pour l'électronique C-MOS hybride
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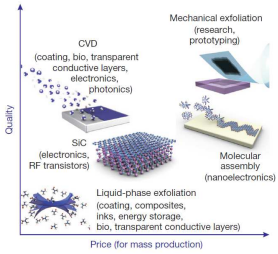
AGENCE NATIONALE DE LA RECHERCHE
ANR

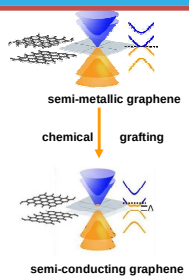
Context



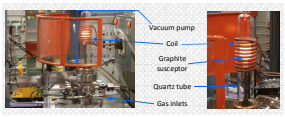
Graphene is a material that has attracted a lot of scientific attention over the past few years as it seems to be compatible with a lot of applications. It can be obtained by various techniques and each technique will provide a graphene with properties better suited for one application rather than another. Regarding the microelectronics field, graphene is an interesting material as it shows ballistic transport and very high mobility; however it is not yet compatible with CMOS-like applications as it lacks a band gap.

The objectives: of the project are to:
- optimize graphene fabrication
- test the functionalization as a tool to tune the graphene band gap

Results presented on
- Task 3: SiC graphene growth
- Task 5: bulk graphene functionalization
- Task 3: suspended graphene

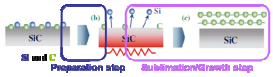


SiC graphene growth

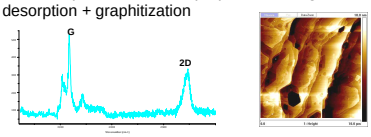


Furnace (induction heating) key aspects: vacuum/inert gas and Ar/H_2 line available

Each growth cycle is decomposed into a preparation step and a sublimation/graphene growth step

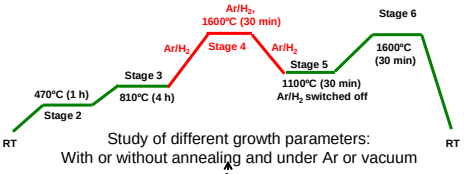


Standard protocol: surface preparation = organic desorption + graphitization

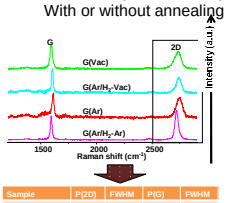


rough samples, small graphene domains

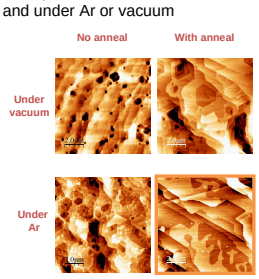
Optimized protocol: surface preparation = idem + H_2 annealing

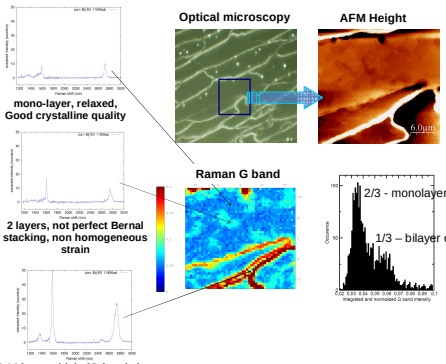


Study of different growth parameters:
With or without annealing and under Ar or vacuum



Sample	P(2D)	FWHM	P(G)	FWHM
G(Vac)	2730.2	62.2	1588.9	24.2
G(Ar)	2743.1	56.4	1605	18.3
G(Ar/H2-Vac)	2737.9	46.3	1598.8	16.9
G(Ar/H2-Ar)	2718.3	31.8	1588.4	16.3





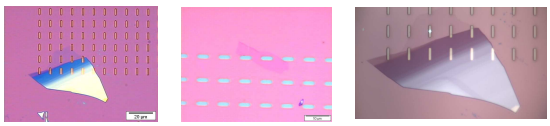
Best graphene sample obtained after H_2 annealing and growth under Ar

Large monolayer domains

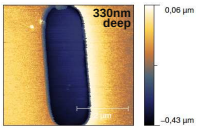
Suspended mechanically exfoliated graphene

Suspended graphene should not show interactions with the substrate. Such type of structure would prevent various parasitic phenomena occurring upon deposition of graphene flakes on SiO_2 (strain, local doping…)

Substrate preparation



Technological steps:
- ✓Starting substrate: SiO_2 (290nm) / Si (100)
- ✓UV projection lithography
  - Metal marks: double resist for undercut + thermal evaporation
  - Pools: normal resist + CF_4 ICP RIE
- ➢Lift-off



5x1 µm² pools: Depths of 160nm, 210nm, 260nm, 340nm already measured (400nm, 480nm, 615nm upcoming)

Graphene Functionalization

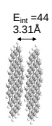
Modification of SiC graphene with CoPc

Samples obtained after immersion of the sample in a CoPc solution in $CHCl_3$ (1' dipping time – concentrations targeted ~10^{-4}M)

Other studies in progress

Theoretical calculations

Graphene model: bilayer more electron donating than monolayer?:



$n_{Cy}(n_c)$ 19 (54)

LUMO -2.87 eV -2.76 eV

HOMO -4.83 eV -4.38 eV

Device fabrication

On exfoliated graphene, with e-beam lithography and thermal evaporation.

Measurements providing:
- -Position of the Fermi level
- -Carrier density
- -Carrier mobility
- -Band gap
- -Corrections to standard conductivity model at low temperature

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